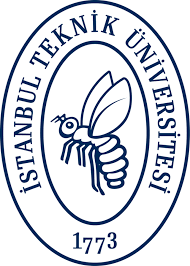
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**VLSI Circuit Design II– EHB 425E**

**HOMEWORK IV**

**Yiğit Bektaş GÜRSOY**

**040180063**

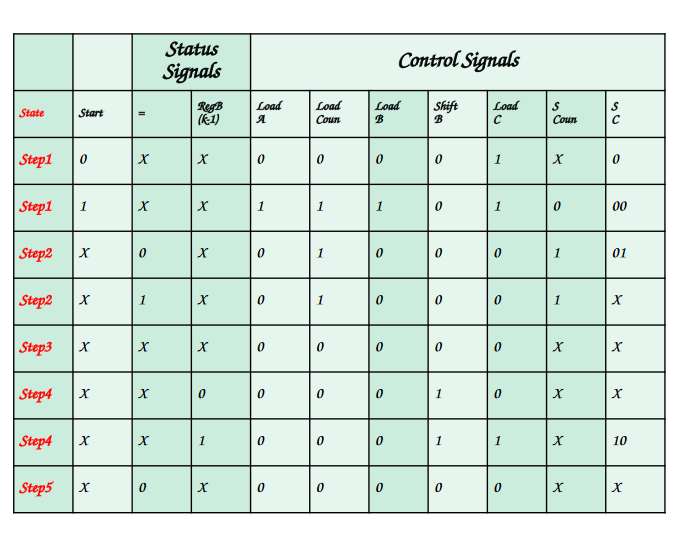
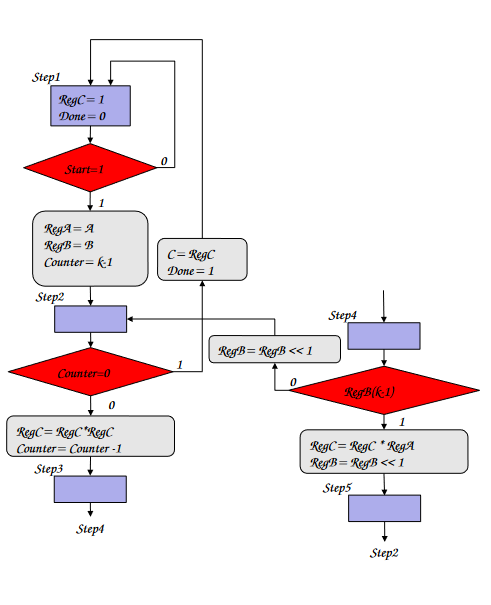
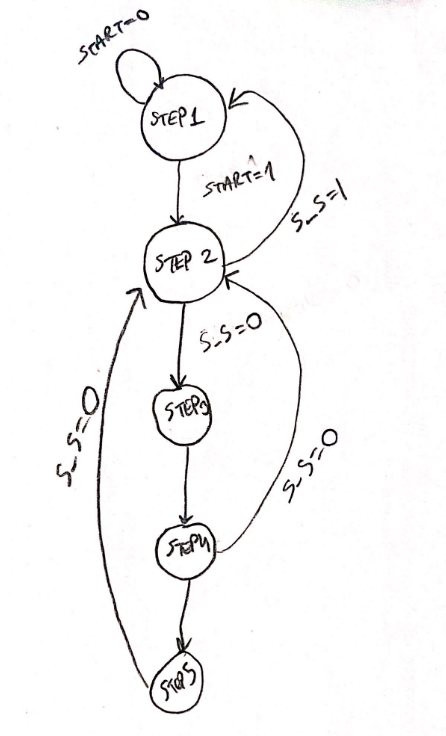
**Class Lecturer: Sıddıka Berna Örs Yalçın**

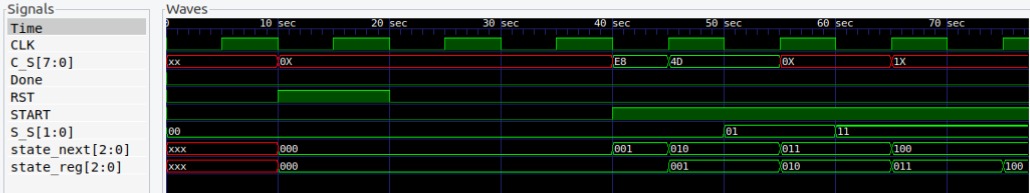
**Class Assistant:  
Yasin Fırat Kula**

1. **Controller**

* **State Diagram**

The state diagram of the figure whose ASM is given below is as shown in the figure. Controller is written according to the diagram in the figure.

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* **GTK Waveform**

As you can see, the code designed according to the state diagram works correctly. The simulation above shows this.

1. **Datapath**

As it was said in the assignment, the datapath was designed based on the k parameter and using the MUL block in HW3. The codes are zipped and put into the assignment file.

* **GTK Waveform**

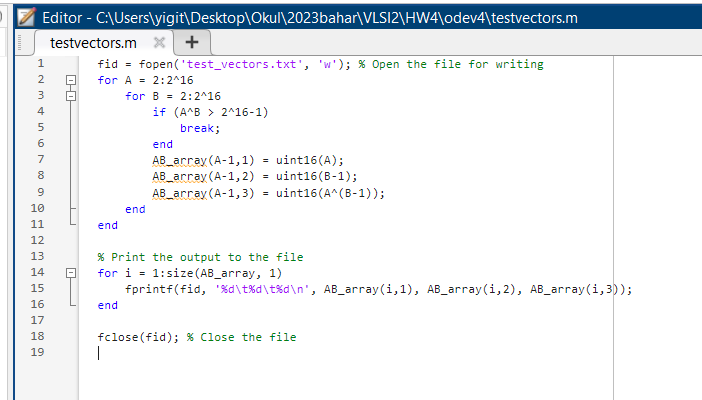


1. **Top Module**

By combining Controller and Datapath, a top module is created.

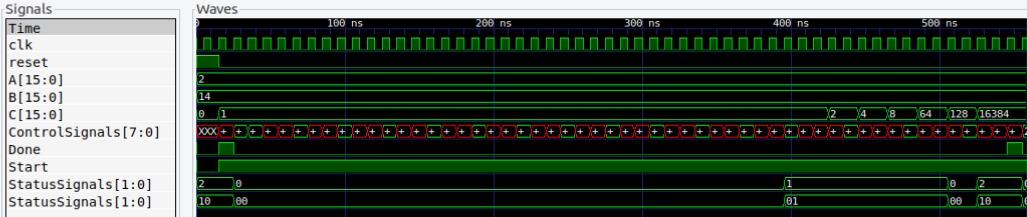
* **MATLAB**

Test vectors were obtained using the following MATLAB code.

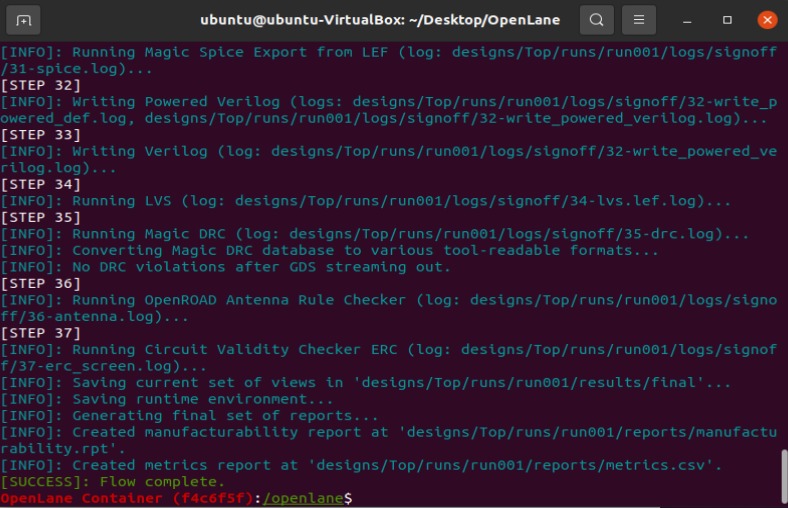
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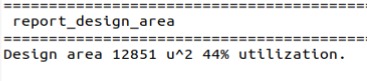
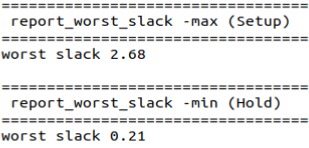
* **GTK Waveform**

where A is the value to be powered. B is the power of A. By looking at the power of 2 here, it can be understood whether the circuit is working correctly. The powers of 2 confirm that the circuit is working correctly. After 2^14 is finally received, the done signal 1 appears to be lit. Indicates that the process is finished.



1. **Openlane Section**

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As can be seen, no errors were encountered while synthesizing. The desired outputs are mentioned above. Max Frequency 🡺 1/6.98\*10^-9 = 143.266 MHz

**All verilog source codes and files with .dot extension are in the archive.**